A RANDOM TRIMMING APPROACH FOR OBTAINING HIGH-PRECISION EMBEDDED RESISTORS

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ABSTRACT

Embedded resistors are resistors fabricated inside of printed circuit boards used as an alternative to discrete resistor components that are mounted on the surface of the boards. However, it is difficult to fabricate embedded resistors to the required resistance value, so embedded resistors are often fabricated with a lower value and then trimmed to raise their resistance to the desired value. A study of embedded resistors containing random voids of varying size and density has been performed. A new trimming strategy in which the trims are made randomly (rather than conventional L-shaped trims) is proposed in this paper. Analysis results demonstrate that single-dive trimming combined with random trimming enables the manufacturing of embedded resistors with higher precision and producibility (C_{pk}) than can be obtained with conventional trimming patterns.

The resistor trimming pattern impacts the distribution of heat in the resistor. Study results show that the highest temperature reached in randomly trimmed NiCr resistors is 7.5% lower than the highest temperature in single-dive trimmed resistors and 1.2% lower than the highest temperature in L-cut trimmed resistors.

1. INTRODUCTION

The world demands a continuous stream of smaller, better performing, and less expensive electronic systems, such as cellular phones. One technology that enables these systems to become smaller and better performing is embedding passives (Ulrich, 2003). Embedded passives are electrical components (most commonly resistors and capacitors) that are fabricated inside or on the surface of printed circuit boards instead of being mounted on them (i.e., "discrete" components).

Embedded resistors are fabricated in one of two ways: 1) subtractive processes – a layer with resistive material plated on it is etched to form specific resistors and then included within the printed circuit board layers, (e.g., Ohmega-Ply; Wang and Clouser, 2001); or 2) additive processes – resistive material is printed or plated onto a layer with other printed circuit board features to form specific resistors, (e.g., D'Ambrisi *et al.*, 2001).

Embedded resistors, however, have several problems that are preventing their widespread adoption. The most serious drawback is that the processes for making resistor geometries (whether subtractive or additive) are inexact, requiring the resistors to be "trimmed" if high precision is required. Resistors are normally fabricated with lower resistance values than required and are trimmed by cutting holes in them with lasers to increase their resistance value (Fjeldsted and Chase, 2002). There are several desirable trimming characteristics: getting as close to the target resistance as possible (precision); minimizing the risk of trimming too much (if a resistor is "over-trimmed," fixing it is impractical, and the entire board that it is in may have to be thrown away); and minimizing the length of each trim (a longer trim takes more time to make and impacts the manufacturing throughput thereby costing more money). Without trimming, embedded resistors can achieve ~10% tolerance (±10% of the target resistance), (Wang *et al.*, 2002; Cheng *et al.*, 2007a; Cheng *et al.*, 2007b), which is insufficient precision for many applications.

Various trimming patterns are used to meet desired trimming characteristics. Common practice is to use "L" shaped trims ("L-cut") (see Figure 1), where a cut perpendicular to the current flow in the resistor quickly increases the resistance to near the target value, then a change in direction of the trim to parallel to the current flow slows down the change in resistance until the trim reaches the target.

Voids (bubbles) in the resistive material complicate the trimming problem, especially for high-precision resistors; if a void is encountered during trimming, the resistance may "jump" uncontrollably to a higher value beyond the target resistance, Figure 2. Although the density and size of voids is a function of the process and materials used to create the embedded resistors, all types of embedded resistors have reported some amount of voiding, e.g., polymer thick-film resistors (Narayana *et al.*, 1992; Chinoy and Langlois, 2004), and thin-film resistors (Snogren, 2004).

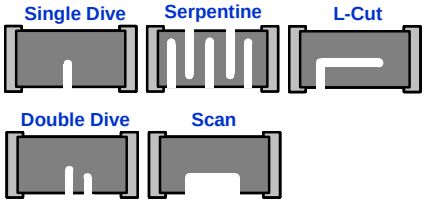

Fig. 1. Common embedded resistor trimming patterns.

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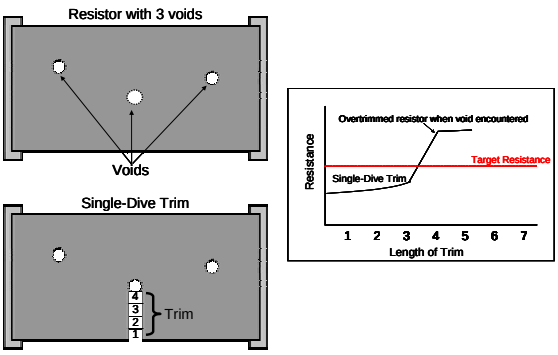

Fig. 2. An embedded resistor containing 3 voids ("bubbles" in the resistive material). If a void is encountered during trimming, the resistance value jumps uncontrollably.

This paper describes an experimental method for emulating embedded resistors, which was used to verify and calibrate a two-dimensional numerical simulation of the embedded resistor trimming process. The model was then used to compare the precision and efficiency of L-Cut trimming patterns with a new random trimming approach applicable to high-precision embedded resistors.

Section 4 addresses the thermal aspects of randomly trimmed embedded resistors. A three-dimensional finite-element model was developed, experimentally verified and used to simulate NiCr embedded resistors. The model was used to determine the location and values of the maximum temperature reached in each resistor.

2. ELECTRICAL EXPERIMENTAL AND SIMULATION METHODOLOGY

An experimental approach that emulated the electrical properties of trimmed embedded resistors was developed and a two-dimensional numerical simulation model was constructed, verified, and calibrated using the experimental results. This section describes both the experimental approach and the simulation model.

2.1 Experimental Approach

To emulate embedded resistors experimentally, trimming of conductive paper was performed (Sandborn and Sandborn, 2007). For a constant sheet resistance (ohms per square), the resistance of a planar resistor does not change with size (i.e., length or width) as long as the ratio of length to width (the aspect ratio) is constant. This relationship is given by,

$$R = \frac{\rho L}{A} = \frac{\rho L}{TW} = \frac{\rho}{T}\left(\frac{L}{W}\right) = R_{\square}\left(\frac{L}{W}\right) \qquad (1)$$

where ρ is the bulk resistivity, A is the cross-sectional area of the resistor, $R_{\square}$ is the "sheet resistance" (in ohms per square), and L, W, and T are the length, width, and thickness of the resistor. From (1) it can be seen that the resistance (R) depends on the ratio of the resistor length and width (rather than the magnitudes of the length and width), therefore, a small planar resistor (dimensions in fractions of millimeters) has the same resistance characteristics as a large area planar resistor (dimensions of centimeters), and trimming of small resistors can be emulated using larger area resistors.

To emulate embedded resistors, sheets of conductive paper (PASCO Scientific, Model Number PK-9025) were cut into 28 x10 centimeter sheets. Silver contacts were added to the two ends of each paper resistor using silver conductive paint. Metal clamps were used to connect to the resistor contacts and ohmmeter probes were connected to the metal clamps. The silver contacts make the resistance measurements less sensitive to the clamp placement or pressure.

The resistance of the conductive paper was found to vary from sheet to sheet. In order to make measurements from multiple sheets comparable, the measurements were normalized. The "normalization" process scaled all untrimmed measurements from each sheet to 65 kΩ. To normalize the various sheets to 65 kΩ, 10-15 initial measurements from each sheet were made prior to trimming, the measurements were averaged, and the average was divided by 65 kΩ to obtain a scaling factor that was specific to the sheet. Every measurement taken from the specific sheet during trimming was multiplied by this scaling factor before comparison with data from other sheets. The normalization process was performed for every resistor used in the experimental study. This normalization procedure accounts for variations in the sheet resistance from sheet-to-sheet only (variations in series resistance in the measurement path are not affected by the normalization, e.g., clamp pressure or placement).

2.2 Numerical Simulation

A numerical simulation of embedded resistors that allows the study of variations in trimming patterns was implemented, calibrated, and verified using the experimental results from trimming conductive paper. Previously reported numerical simulations of trimmed embedded resistors include: models for predicting the performance of laser-trimmed resistors taking into account the heat-affected zone around the trim (Ramirez-Angulo *et al.*, 1987; Ramirez-Angulo and Geiger, 1988); numerical trim simulations that were used in the resistor design process to predict trim results (Schimmanz and Jacobson, 2002; Poslethwaite, 1984; Schimmanz and Kost, 2004); and three-dimensional simulators that were utilized in modeling electronic interconnect structures, (Martins *et al.*, 1998). The model developed here is a finite difference model formulated similarly to Ramirez-Angulo *et al.* (1987) and is described in this section.

A grid is superimposed on the resistor. The resistor is assumed to be uniform in the third dimension (into the board), in order to isolate the two-dimensional problem. To determine the resistance of the embedded resistor, the voltage at each of the grid points must first be determined. The voltage is found by solving Laplace's Equation in two dimensions at each grid point,

$$\nabla^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0 \qquad (2)$$

where V is the voltage. Assuming that the distances between the grid points in the plane of the resistor are the same, a 5-point finite difference approximation of Laplace's Equation reduces to,

$$V_{i,j-1} + V_{i-1,j} - 4V_{i,j} + V_{i+1,j} + V_{i,j+1} = 0 \qquad (3)$$

An equation like the one above is written for every grid point. The system of equations is solved by writing the set of equations in the form of a matrix equation. A Gaussian Elimination technique is then used solve the matrix equation for the voltages at every point.

Once the voltages at all the points have been solved for, the electric field ($\overline{E} = -\nabla V$) at every point can be found by differencing, and the current density at every point is given by,

$$\overline{J} = \sigma \overline{E} = \frac{\overline{E}}{R_{\square}} \qquad (4)$$

where σ is the conductivity and $R_{\square}$ is the resistivity (Ω/□) of the material. Using Ohm's Law, the resistance is,

$$R = \frac{V_{applied}}{\sum_{\gamma} J_x \Delta y} \qquad (5)$$

where γ is any line connecting the top and bottom (non-contact edges) of the resistor and Δy is the grid spacing in the non-contact direction.

On the contact ends of the resistor, the voltage is known (Dirichlet boundary condition). On the top and bottom of the resistor, the electric field perpendicular to the boundary is zero (Neumann boundary condition),

$$\overline{E} = -\nabla V = -\frac{\partial V}{\partial x}\hat{x} - \frac{\partial V}{\partial y}\hat{y} \qquad (6)$$

so, at the top and bottom boundary (y is perpendicular the top and bottom),

$$E_y = -\frac{\partial V}{\partial y} = 0 \qquad (7)$$

Trims into the resistor and voids in the resistive material require applying a Neumann boundary condition on the edges of the trim or the void.

The simulator was verified against experimental results using conductive paper by both probing the voltage in the resistor and measuring the resistance as a function of trimming the resistor, Figure 3. The trim spot size in the simulator also had to be calibrated. This was performed by experimentally trimming one spot successively larger in an experimental resistor sheet until the resulting resistance matched the resistance on a 1 x 1 grid cell trimmed in the simulator.

3. RESULTS: TRIMMING ANALYSIS

Random trimming is performed by choosing a point on the resistor at random, and then "firing" a hole into that position, Figure 4. Random trimming by itself, although well controlled, is generally too long of a process (it takes too much time). So, random trimming was combined with the single-dive trim in the following way: a single-dive was performed to reach a target resistance range quickly, and then the random trim was implemented to get as close to the target resistance as possible. If a random trim happens to coincide with or touch a void, the effect on the resistance is intuitively much less than it would be if a void is encountered on the edge of one of the fixed trimming patterns shown in Figure 1. It was also necessary to define the current channel region between the end of the single-dive and the edge of the resistor as an area where random trims were not allowed in order to better control the resistance.

Note, the random trimming approach suggested herein differs from the "swiss cheese" approach suggested in Ramirez-Angulo and Geiger (1988), where a set of trim targets are initially created as holes in the resistor and then cuts from the edge of the resistor to the targets are performed. In the random trimming approach proposed here, after an initial single-dive trim into the resistor, random trims are made. This approach decreases the heat-affected portion of the resistor and provides a controlled approach to the target resistance that minimizes the sensitivity of the trim to voids that may be present in the resistor material. The following sections quantify the performance and producibility (process capability) of random trimming relative to L-cuts.

3.1 Trimming Precision Results

For the example shown in Figure 5, the target resistance was 100 kΩ. When trimming with a single-dive, the resistance increase per trim step near the target

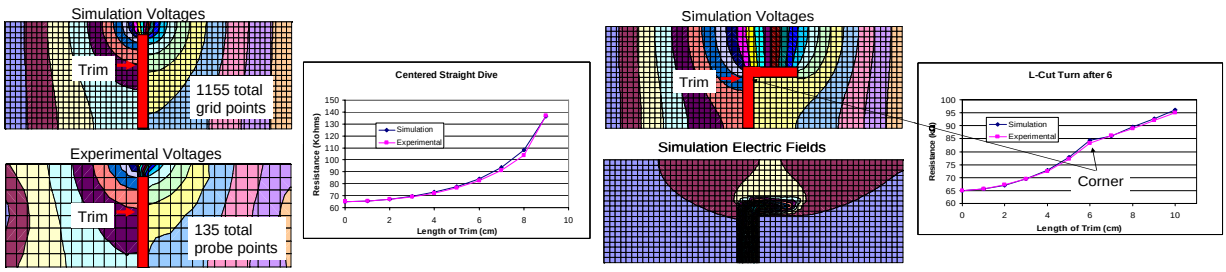

Fig. 3. Simulation verification for a single-dive and an L-cut trim by comparison with experimental results. This figure includes contour plots that show the voltage variations and electric field variations.

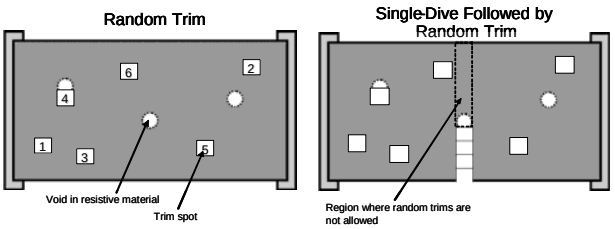

Fig. 4. Random trimming. Left – pure random trimming; right – single-dive first then random trim to target. Example voids are also indicated.

was 3.8 times greater than that of an L-cut, and 15 times greater than that of a random trim. This result demonstrates that the random trim results in a significant increase in precision compared to the single-dive and L-cut. If the trimming pattern can get closer to the target, a higher precision resistor can be fabricated. Higher precision trimming allows a larger fraction of the resistors in a system to be embedded (as opposed to discrete).

The result in Figure 5 is an example for a single resistor without voids. To statistically demonstrate random trimming's precision advantages, trimming was performed on resistors with a range of void densities (1-6 voids per resistor) and void sizes in the 28 x10 centimeter resistors (4 different void diameters: 1.0 centimeter, 1.5 centimeters, 2.0 centimeters, and 2.5 centimeters).

The following steps were performed to obtain quantitative results from the numerical simulation: for a resistor with a specific number of voids of a specific size: 1) randomly place the voids in the resistor, 2) perform a single-dive to a specific depth (specified percentage of target resistance), and 3) perform either an L-cut (conventional approach) or random trim (proposed new approach) to reach the target resistance. Steps 2 and 3 were then repeated for a series of random void placements. The whole process was repeated for a range of void densities (voids per resistor) and void sizes.

Analyses were performed by varying the stopping criterion for the single-dive. Figure 6 shows an analysis for initial single-dive depths ranging from 82.5% of the target to 93.4% of the target. If the single-dive was allowed to go as far as possible without over-trimming (which can be done with the simulation, but would be impractical for real resistors; not shown on Figure 6) random trimming reduces the mean error after trimming from 1.8% for L-cuts to 0.46%.

The result in Figure 6 shows that the precision obtained from L-cuts decreases as the initial single-dive goes further into the resistor; however, the precision that can be obtained from the random trim is approximately independent of the length of the initial single-dive. Figure 6 also shows distributions of the L-cut precision and the random trim precision. The shapes of the distributions shown in Figure 6 allow the inference to be made that the precision of random trimming may be, for practical purposes, better than the calculated mean.

The result in Figure 7 shows that the number of trimming steps necessary to reach the target decreases as the initial dive depth increases and is always larger with random trimming (as would be expected). However, the result in Figure 7 suggests that the single-dive/random trimming combination can be practically used with an initial dive depth of 93.4% while L-cuts are probably practically limited to an initial dive depth of 87% or less.

3.2 Process Capability (Producibility) Results

The previous section addresses how close the L-cut and random trimming approaches can get to a target resistance ("precision"), but it does not address the capability of the trimming process to produce embedded resistors that fall into an application's specification range, e.g., the ability to obtain a 1% or 5% resistor.

The calculation of C_{pk} will be used to examine the spread as well as the centricity of a process between specification limits.

$$C_{pk} = \frac{\min[HSL - \mu, \mu - LSL]}{3\sigma} \qquad (8)$$

where HSL and LSL are high-specification limit and low-specification limit respectively, μ is the mean of the process, and σ is the standard deviation.

An analysis of the C_{pk} for the random trimming process was performed, and was compared with the C_{pk}

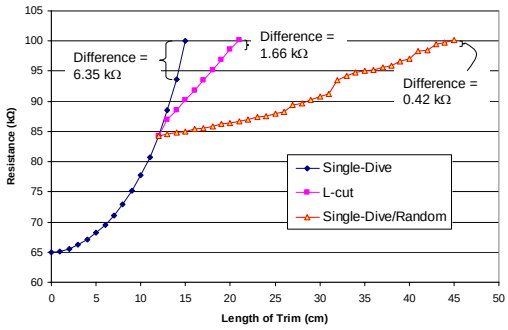

Fig. 5. Random trimming allows a significant increase in precision compared to the single-dive and L-cut in a resistor without voids. (Resistor dimensions: 28 cm x 10 cm, dimensions similar to that of conductive paper)

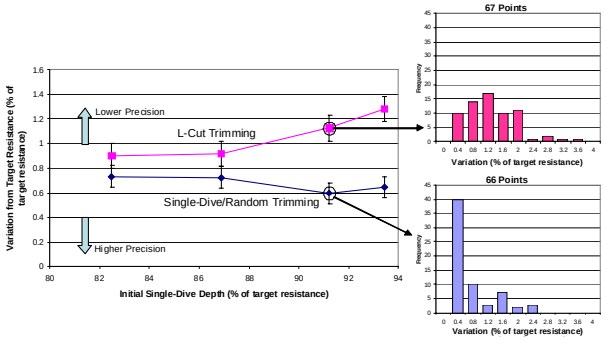

Fig. 6. Trimming precision as a function of stopping criteria. Each data point in the graph on the left represents the mean of 55 or more void density/void size combinations. The histograms on the right show the data from two of the points.

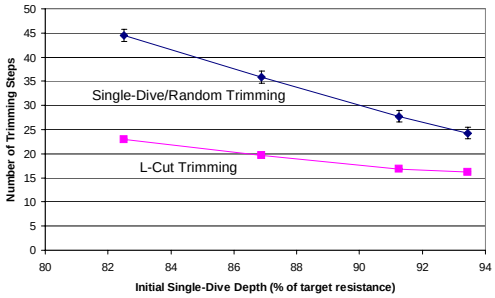

Fig. 7. Number of trim steps necessary to reach the target resistance. Each data point represents the mean of 55 or more void density/void size combinations.

for the L-cut trimming process. Sets of 200 resistors with similar void characteristics were defined for each trimming process, random and L-cut. Each resistor was trimmed past a target of 38 kΩ and the resistance was measured after each successive trim step. The mean and standard deviation used in the C_{pk} calculation were derived from the absolute values of resistance steps that were closest to the target of 38 kΩ. Figure 8 shows the L-cut trimming and random trimming processes with the target of 38 kΩ and a required design tolerance of ±0.78%. C_{pk} values for this scenario (4 randomly placed voids with 2 centimeter diameter and ±0.78% tolerance – these simulations emulate the conductive paper resistors, see Section 2.1) were calculated as approximately 0.54 for the random trimming process and about 0.37 for the L-cut trimming process (higher C_{pk} is better).

C_{pk} values for L-cut and random trimming processes vary with different void characteristics. For example, for 2.5% tolerance resistors, the C_{pk} for the random trimming process in the presence of two randomly placed voids was 2.40, where the C_{pk} for the L-cut trimming process was calculated to be 1.98. Fjeldsted and Chase experimentally determined C_{pk} values ranging from 2.4 to 3.0 for resistors trimmed to within 1% tolerance using the L-cut (Fjeldsted and Chase, 2002). These measured C_{pk} values are larger than the simulated values obtained here, but the trim step sizes and voiding characteristics are not known for the measured results (i.e., if the material had fewer or relatively smaller voids, or the effective step size was smaller, higher C_{pk} would be expected).

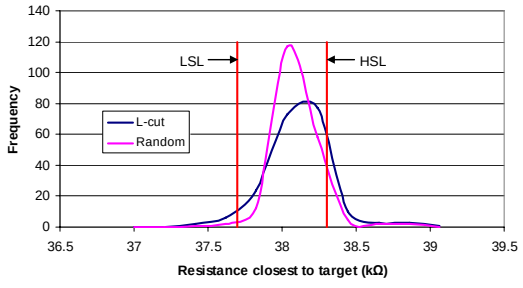

Fig. 8. Process capability for L-cuts and random trims, with target at 38 kΩ and tolerance of ±0.78%. The "low specification limit" (LSL) is 37.7 kΩ (-0.78% of target), and the "high specification limit" (HSL) is 38.3 kΩ (+0.78% of target).

4. THERMAL ANALYSIS

One problem with embedded resistors is that they dissipate energy in the form of heat. Inserting heat generating elements inside of printed circuit boards is generally detrimental to the reliability of the board. Heat generated inside of printed circuit boards may accelerate board failure mechanisms that are associated with delamination of the board's layers.[1]

For a resistor of a given value, the total power dissipated (P) by the resistor is,

$$P = I^2 R = \frac{V^2}{R} \tag{9}$$

where I is the current flowing through the resistor, R is the resistance value of the resistor, and V is the voltage across the resistor.

The total power dissipated by the resistor is only dependent on the final value of its resistance and the voltage applied across the resistor; power dissipation is not dependent on how the resistor is trimmed. However, the distribution of heat in the resistor is dependent on the trim pattern.

From a board reliability viewpoint, the ideal embedded resistor would not have to be trimmed at all: resulting in the power dissipated by the resistor being evenly distributed throughout the resistive material. However, trimming a resistor causes a non-uniform current density in the resistor. As a result, the power dissipation is non-uniform, which means that some locations in the resistor are hotter than other locations. For board (and resistor) reliability reasons, it is advantageous to design resistors that minimize hot spots and distribute the heat generated as uniformly as possible.

4.1 Modeling Resistor Temperatures

Unlike the electrical analysis of embedded resistors, which was well approximated by a two-dimensional model (see Section 2.2), a thermal analysis must be performed in three-dimensions since heat is dissipated from the resistor in the out-of-plane dimension.

The temperature as a function of location in an embedded resistor can be simulated by solving the heat diffusion equation,

$$\nabla^2 T = \frac{C_p d}{k}\frac{\partial T}{\partial t} + \frac{q_{gen}}{k} \tag{10}$$

where C_p is specific heat capacity, d is density, k is thermal conductivity, T is temperature, q_{gen} is power generation per unit volume, and t is time. A steady-state analysis is of interest in this study, therefore the time derivative on the right hand side of (10) is zero.

[1] Note, not every resistor in an application is embedded – resistors that dissipate large amounts of power are usually not candidates for embedding.

The heat diffusion partial differential equation can be converted to a system of ordinary differential equations by means of the finite-element method. ANSYS was used to perform the finite-element modeling for heat diffusion in an embedded resistor. The models were generated using the ANSYS SOLID69 element type since it allows for a coupled electrical and thermal analysis. Material properties for the simulation were matched to the NiCr resistors described in Wang *et al.* (2003), Table I.

Table I
NiCr Resistor Material Properties (Wang *et al.*, 2003).

Electrical Resistivity (Ω-m)	0.00016
Thermal Conductivity (W/mK)	70
Material Thickness (m)	3.2x10-7

When embedded, a resistor is laminated between two insulating layers such as FR4. During operation, resistors dissipate heat via conduction into these FR4 layers, which in turn dissipate heat via convection into the air flowing around the printed circuit board. The embedded resistor was modeled in three dimensions; however, the layers above and below the resistor were modeled with an effective film coefficient instead of a detailed, three-dimensional model of the layers (see the Appendix). The assumption of an effective film coefficient is valid as long as the spreading of heat laterally in the printed circuit board layers is minimal.

The effective film coefficient for the model was determined by comparing model results with data from Wang, *et al.* (2003). An ANSYS simulation of a 30 mil x 30 mil (1 mil = 1/1000 inch) NiCr resistor dissipating 20 W/in^2 with a bias voltage of 3 volts was used. Results from Wang, *et al.* (2003), indicate a maximum temperature of 130 °C was reached in the resistor. The effective film coefficient in the ANSYS simulation was adjusted to match this maximum temperature - a film coefficient of 145 W/m^{2}K was determined. Figure 9 shows the maximum temperature reached in untrimmed NiCr resistors analyzed by Wang, *et al.* (2003), and results from the calibrated ANSYS model for various power densities (obtained by varying the bias voltage).

The thermal model for embedded resistors was experimentally verified by measuring the temperature distribution in resistors cut from resistive paper. To measure the temperatures, 1000 volts was placed across the paper and a J-type thermocouple was used to probe the surface of the paper.[2]

Figure 10 shows temperatures from experimental and modeled resistors. The distributions of contours demonstrated on the experimental results and the

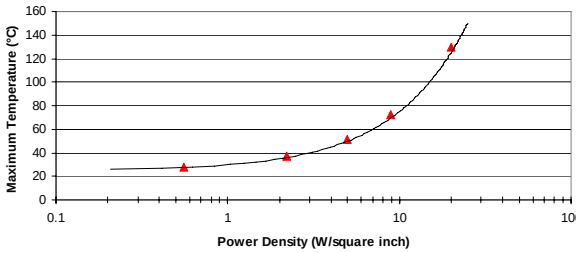

Fig. 9. Maximum temperature reached in untrimmed NiCr resistors. The line represents data collected by Wang, *et al.* (2003); all the data points are results from this study's ANSYS simulation of NiCr resistors using an effective film coefficient of 145 W/m^{2}K.

distribution of heat in the same resistors from simulation agree qualitatively. On the left side of Figure 10 (a random trimming variation: "single-dive/random trimming"), several hot spots are noticeable in both the experiment and model. It is also important to note that the experimental temperatures vary because the contacts in the experimental method do not span the entire width of the resistor, whereas in the model they do. This results in a heat spreading effect that is evident in both experimental cases (the center of the right and left edges are hotter than the upper and lower portions).

4.2 Thermal Modeling Results

Other authors have modeled the thermal aspects of embedded resistors (Ramirez-Angulo and Geiger, 1988; Martins *et al.*, 1998; Wang *et al.*, 2003; Stubbs *et al.*, 2000). Ramirez-Angulo and Geiger (1988), studied the "heat affected zone" in trimmed resistors, specifically changes in the resistor's sheet resistance, thermal conductivity, and aging behavior caused by a laser trimming process. Similar to Ramirez-Angulo and Geiger (1988), Martins, *et al.* (1998), modeled the heat affected zone in resistors trimmed with single-dives and L-cut variations. Wang, *et al.* (2003) and Stubbs, *et al.* (2000) studied the thermal management of printed circuit boards that contain embedded resistors. Previous studies have not addressed the maximum temperature reached in trimmed resistors and not studied the random trimming.

In order to determine the effects of random trimming on the heat dissipation in embedded resistors, NiCr resistors with different trimming patterns were compared to determine the highest temperature in each resistor.

An analysis strategy was performed for resistors trimmed with different patterns, but all resulting in the same resistance. One case each of a single-dive trimmed resistor and an L-cut trimmed resistor was modeled. Only one case was necessary for these trims because there was no variation in the pattern. 30 unique single-dive/random trimming cases were modeled, each with the same resistance as the single-dive and L-cut cases.

[2] Determining temperatures by probing the surface of the paper with a thermocouple is not an ideal approach because the thermocouple provides a heat-conduction path away from the paper, however, the thermocouple tip was very small and the primary objective of the experimental verification was to determine the location of the highest temperature in the resistor.

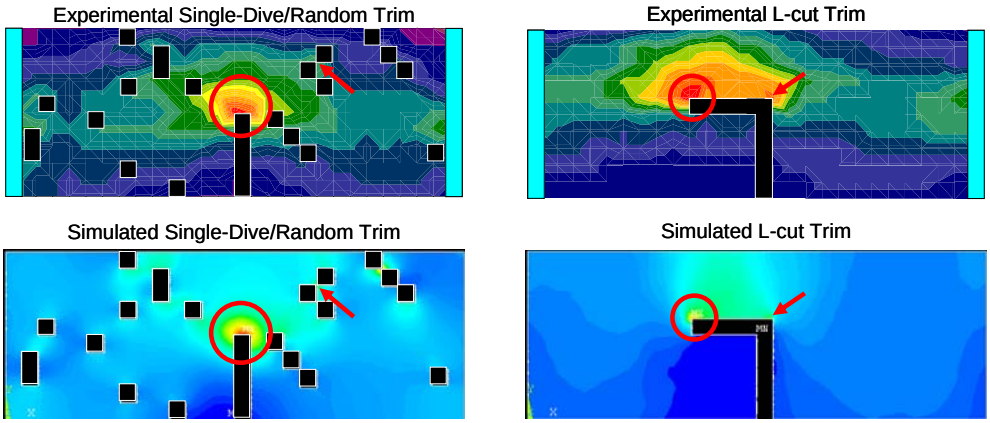

Fig. 10. Temperature distributions from experiment and simulation. Contour coloring not consistently scaled in each plot.

Each case was evaluated using the thermal model described in Section 4.1, and the highest temperature was recorded. Figure 11 shows the highest temperatures reached in resistors trimmed using random trimming, the single-dive/random trimming combination, the L-cut, and the single-dive. The distribution of random trimming cases is centered at an average of 33.30 °C, with a standard deviation of 0.58 °C. The distribution of single-dive/random trimming cases is centered at an average of 34.18 °C, with a standard deviation of 0.36 °C. The highest temperature reached in the L-cut case was 35.26 °C, and the highest temperature reached in the single-dive case was 35.60 °C.

5. DISCUSSION AND CONCLUSIONS

A study of embedded resistors with random voids of varying size and density was performed. A new trimming strategy in which the trims are made randomly (rather than conventional L-shaped trims) has been proposed and the results of the analysis demonstrate that single-dive trimming combined with random trimming allows higher precision embedded resistors to be obtained than conventional trimming patterns. Table II indicates that a 29% increase in precision can be obtained for a 17% increase in the number of trim steps. Simulated capability indices show that when compared to conventional L-cut trimming, the random trimming process increases C_{pk} for 1% resistors from 0.83 to 1.00 and for 5% resistors from 3.96 to 4.80. The results in this paper suggest that the single-dive/random trimming combination is a potentially better way to trim embedded resistors than conventional L-cut trimming when high precision is required. This work provides a manufacturing improvement that enables applications to potentially embedded a greater fraction of their resistors within printed circuit boards leading to possible electronic system size and cost reductions.

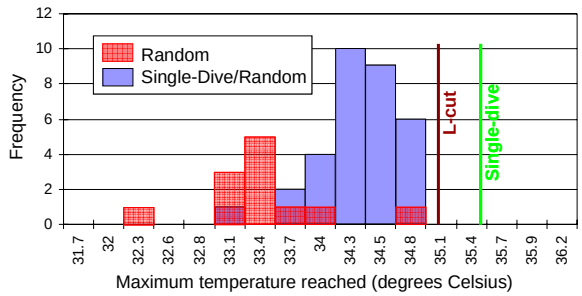

Fig. 11 Maximum temperatures reached in resistors trimmed using a single-dive, L-cut, a single-dive/random trimming combination, and "pure" random trimming.

Table II
Comparing the Highest Precision L-cut to the Most Efficient Single-dive/Random Trim

	Initial single-dive depth as % of target (Fig. 10)	Number of trimming steps to target (Fig. 11)	Precision as % deviation from target (Fig. 10)
Highest Precision L-cut	87%	20	0.92%
		Δ = 17%	Δ = 29%
Most efficient single-dive/random trim	93.4%	24	0.65%

Randomly trimmed resistors were compared with conventionally trimmed resistors to determine the effects of random trimming on the temperature distribution in the resistor. The analysis described in this paper demonstrates that single-dive trimming combined with random trimming reduces the maximum temperature in an embedded resistor when compared with resistors trimmed using the L-cut or single-dive trimming patterns.

Finite-element modeling of embedded resistors was qualitatively verified against measurements performed on resistive paper. The locations of relatively warm and cool spots were the same in both the model and experiment. A quantitative verification of the model was not possible because the thermal conductivity of the resistive paper was not known, and varies from paper to paper.

Finite-element modeling of NiCr resistors shows that the single-random trimming combination reduces the maximum temperature reached in an embedded resistor from 35.26 °C for L-cuts to 34.18 °C, a difference slightly greater than 1 °C. "Pure" random trimming reduces the maximum temperature reached to 33.30 °C. Although the maximum temperatures in the randomly trimmed resistors are smaller than that of the L-cut, the temperature

differences are relatively small and the impact on the reliability of the board is most likely minimal.

APPENDIX – EFFECTIVE FILM COEFFICIENT

This appendix discusses the use of an effective film coefficient to represent the layers above and below the embedded resistor. Heat flows out of the top and bottom (out-of-plane) surfaces of a resistor via conduction into the layers above and below. In turn, heat flows out of these layers via convection into air.

The heat flow by conduction between two points separated by Δx, $Q_{conduction}$, is given by,

$$Q_{conduction} = kA\frac{\Delta T}{\Delta x} \quad (A.1)$$

where k is the thermal conductivity, A is the cross-sectional area, and ΔT is the temperature change between the two points. The heat flow by convection between two points, $Q_{convection}$, is given by,

$$Q_{convection} = hA\Delta T \quad (A.2)$$

where h is the heat transfer coefficient, A is the cross-sectional area, and ΔT is the temperature difference between the two points. An alternative equation for heat flow, Q, can be used which incorporates "thermal resistance," R,

$$Q = \frac{\Delta T}{R} \quad (A.3)$$

Using (A.1)-(A.3), the conductive, $R_{conduction}$, and convective, $R_{convection}$, thermal resistances are,

$$R_{conduction} = \frac{\Delta x}{kA_{conductive}}, \quad R_{convection} = \frac{1}{hA_{convective}} \quad (A.4)$$

In the case shown in Figure 14, Δx is the thickness and k is the thermal conductivity of the printed circuit board material above or below the embedded resistor, and $A_{conductive}$ is the area through which conduction takes place. $A_{convective}$ is the area through which convection takes place, and h is the heat transfer coefficient associated with the air above or below the printed circuit board. The total thermal resistance, R_{total}, to ambient assuming identical parallel paths for heat flow above and below the board in Figure 11 is given by,

$$R_{total} = \frac{1}{2}(R_{conduction} + R_{convection}) = \frac{R_{effective\ convection}}{2} = \frac{1}{2h_{effective}A} \quad (A.5)$$

If $A_{conduction} \approx A_{convection} \approx A$, then the effective film coefficient, $h_{effective}$, is given by,

$$\frac{1}{h_{effective}} = \frac{xA}{kA_{conduction}} + \frac{A}{hA_{convection}} \approx \frac{x}{k} + \frac{1}{h} \quad (A.6)$$

REFERENCES

Cheng, P., Leung, S., Law, T., Liu, C., Chong, J. and Lam, D., 2007a: Quantitative Analysis of Resistance Variations in Nickel-Phosphorus (NiP) Resistors, *IEEE Trans. on Components and Packaging Tech.*, **30**(2) 264-268, June.

Cheng, P., Leung, S., Law, T., Liu, C., Chong, J. and Lam, D., 2007b: Quantitative Analysis of Resistance Tolerance of Polymer Thick Film Printed Resistors, *IEEE Trans. on Components and Packaging Tech.*, **30**(2) 269-274, June.

Chinoy, P. and Langlois, M., 2004: Thin-Film Embedded Resistor and Capacitor Technologies, *Circuit World*, **30**(1), 16-19.

D'Ambrisi, J., Fritz, D. and Sawoska, D., 2001: Plated Embedded Resistors for High Speed Circuit Application, *Proc. IPC Annual Meeting*, October.

Fjeldsted K. and Chase, S., 2002: Embedded Passives: Laser Trimmed Resistors, *CircuiTree*, 70-76, March.

Martins, R., Pyka, W., Sabelka, R. and Selberherr, S., 1998: "High-Precision Interconnect Analysis, *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, **17**(11), 1148-1159, Nov.

Narayana, T. Ramkumar, K. and Satyam, M. 1992: Mechanism for Downward Trimming of Polymer Resistors, *J. Phys. D: Applied Phys*., **25**, 717-721.

Postlethwaite, B., 1984: CAD Simulations Improve Resistor Trimming Results, *Hybrid Circuits*, 100-105, June.

Ramirez-Angulo, J. and Geiger, R., 1988: New Laser-Trimmed Film Resistor Structures for Very High Stability Requirements, *IEEE Trans. on Electron Devices*, **35**(4), 516-518, April.

Ramirez-Angulo, J., Geiger, R. and Sanchez-Sinencio, E., 1987: Characterization, Evaluation, and Comparison of Laser-Trimmed Film Resistors. *IEEE J. of Solid-State Circuits*. **SC-22**(6), 1177-1189, December.

Schimmanz, K. and Jacobson, S., 2002: Film Resistor Design for High Precision Laser Trimming," Preprint BTU-Cottbus M-02/02, Germany.

Schimmanz, K. and Kost, A., 2004: BEM Simulation of Laser Trimmed Hybrid IC Resistors, *Int. J. of Appl. Electromagnetics and Mech.*, 19(1-4), 253-256.

Ohmega-Ply, www.ohmega.com.

Sandborn, P. and Sandborn, P., 2007: Using Embedded Resistor Emulation to Teach Measurement Methods and Associated Engineering Model Development, *International Journal of Engineering Education*, **23**(4), 834-840.

Snogren, R., 2004: "Designing Resistors to Embed," *Proceedings of IPC Works*.

Stubbs, D., Pulko, S., Wilkinson, A., Wilson, B., Christiaens, F. and Allaert, K., 2000: Embedded Passive Components and PCB Size – Thermal eEfects," *Microelectronics International*, 17(2), 7-10.

Ulrich, R. and Schaper, L., 2003: *Integrated Passive Component Technology*, Wiley-IEEE Press.

Wang, G., Barlow, F. and Elshabini, A., 2002: "Modeling and Control of Resistance Tolerance for Embedded Resistors in LTCC, *Proceedings of the Electronic Components and Technology Conference*, 516-525.

Wang, J. and Clouser, S., 2001: Thin Film Embedded Resistors, *Proc. IPC Expo*, S08-1-1, April.

Wang, J., Davis, M., Hilburn, R. and Clouser, S., 2003: Power Dissipation of Embedded Resistors, *Proceedings of IPC Printed Circuits Expo*, Long Beach, CA, 23-27, March.